

What is Claimed is:

1 1. During the testing of the operation of processing
2 unit, a system for identifying the occurrence of a new
3 secondary code execution start point condition in the
4 pipeline flattener, the system comprising:
5 timing trace apparatus responsive to signals from the
6 processor unit, the timing trace apparatus generating a
7 timing trace stream;
8 program counter trace apparatus responsive to signals
9 from the processing unit, the program counter trace
10 apparatus generating a program counter trace stream; and
11 synchronization apparatus applying periodic signals to
12 the timing trace apparatus and to the program counter trace
13 apparatus, the periodic signals resulting in periodic sync
14 markers in the timing trace stream and in the program
15 counter trace stream.
16 wherein the program counter trace apparatus is
17 responsive to a new secondary code execution start point
18 signal, the program counter trace apparatus generating a
19 sync marker signal group identifying the occurrence of the
20 new secondary code execution start point signal and
21 relating the beginning of new secondary code execution
22 start point to the timing trace stream and to the program
23 code execution.
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1 2. The system as recited in claim 1 wherein the
2 marker signal group includes a program counter address, a
3 timing index and a periodic sync ID.

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5 3. The system as recited in claim 1 further
6 comprising:

7 data trace apparatus responsive to signals from the
8 processing unit, the data trace apparatus generating a data
9 trace stream, wherein the periodic signals are applied to
10 the data trace apparatus resulting in periodic sync markers
11 in the data trace stream; and

12 a host processing unit, the host processing unit
13 responsive to the timing trace stream, the program counter
14 trace stream and the data trace stream, the host processing
15 unit reconstructing the processing activity of the
16 processing unit from the trace streams.

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18 4. The method for communicating an occurrence of a
19 new secondary code execution start point signal from a
20 target processor unit to a host processing unit after
21 return from an original secondary code execution sequence,
22 the method comprising:

23 generating a timing trace stream, a program counter
24 trace stream, and data trace stream, and

25 in the program counter trace stream, including a
26 program code start point sync marker signal group
27 indicating an occurrence of a new secondary code execution

1 start point signal and relating the signal occurrence to
2 the data trace stream and to the timing trace stream.

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4 5. The method as recited in claim 4 further
5 including:

6 including periodic sync markers in the timing trace
7 stream and in the program counter trace stream; and

8 including in the new secondary code execution start
9 point sync marker reference to a periodic sync marker.

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11 6. In a processing unit test environment wherein a
12 target processor transmits a plurality of trace streams to
13 a host processing unit, a new secondary code execution
14 start point sync marker signal group in a trace signal
15 stream, the marker signal group comprising:

16 indicia of the occurrence of a new secondary code
17 execution start point signal;

18 indicia of the relationship of the occurrence of the
19 new secondary code execution start point signal to the
20 target processor clock; and

21 indicia of the relationship of the occurrence of the
22 new secondary code execution start point signal to the
23 target processor program execution.

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25 7. In a target processing unit generating trace test
26 signals for transfer to a host processing unit, a program
27 counter trace generation apparatus comprising:

1 sync marker assembly apparatus, the sync marker
2 assembly apparatus including:

3 a storage unit;

4 a decoder unit responsive to a new secondary code
5 execution start point signal for storing an indicia of the
6 new secondary code execution start point signal in the
7 storage unit, the decoder unit generating a control signal;
8 a gate unit having a timing index, a periodic
9 sync signal, and a program counter address, the gate unit
10 storing the timing index, the periodic sync signal and the
11 program counter address in the storage unit in response to
12 the control signal; and

13 a FIFO unit, the storage unit transferring the
14 stored signals to the FIFO unit in the form of a program
15 code start point sync marker.

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17 8. The program counter trace apparatus as recited in
18 claim 7 responsive to a selected control signal for
19 transferring the new secondary code execution start point
20 sync marker in the FIFO unit to an output port of the
21 target processor.

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23 9. The program counter trace apparatus as recited in
24 claim 8 wherein the apparatus can form a periodic sync
25 marker in response to a periodic sync signal.

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1 10. The program counter trace apparatus as recited in
2 claim 9 wherein the new secondary code execution start
3 point signal indicates the change from a first instruction
4 code sequence to a second instruction code sequence exiting
5 the pipeline flattener.

6
7 11. The program counter trace apparatus as recited in
8 claim 10 wherein the first instruction code sequence is an
9 original interrupt service routine code and the second
10 instruction sequence is a new interrupt service routine.
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